REMARKS

Applicant has amended the claims to better define the present invention, Applicant acknowledges allowability of claims 5, 6 and 16-20.

The claims now still being prosecuted are claims 1-4 and 7-15.

In the Final Office Action dated October 28, 2003, claims 1, 2 and 7-15 were rejected under 35 USC §102(e) as anticipated by **Sakamoto** (USP 6,387,768); and claims 3 and 4 were rejected as obvious under 35 USC §103(a) in view of a combination of **Sakamoto** and **Saito et al.** (USP 6,537,369). Reconsideration and removal of these rejections are respectfully requested in view of the present amendments to the claims and the following remarks.

With respect to claims 1, 2 and 7-15, the Final Office Action states that both layers 910 and 1810 of **Sakamoto** are outgoing base electrodes, because the layers 910 and 1810 are comprised of the same materials and perform the same functions.

However, as now clearly pointed out in the claims, only a base layer is connected to a first semiconductor layer in a base region of the present claimed semiconductor device.

On the other hand, in **Sakamoto**, the side wall portion 1810 is connected to the first semiconductor layer (n-type epitaxial layer) 210 through a dopant forming region 1820. That is, in **Sakamoto**, not only a base layer 1910 but also the side wall portion 1810, through the dopant forming region 1820, is connected to the first semiconductor layer 210.

Therefore, the present invention is clearly distinct from and unobvious in view of **Sakamoto**.

In the present invention, since only the base layer is connected to the first semiconductor layer

in the base region, it is possible to provide a semiconductor device with a small parasitic capacitance between the base and the first semiconductor layer. Therefore, in the present invention, it is possible to provide a semiconductor device having high speed operation.

In **Sakamoto**, however, since the side wall portion 1810 is connected to the n-type epitaxial layer 210 through the dopant forming region 210 through the dopant forming region 1820, a parasitic capacitance between the base and the n-type epitaxial layer 210 is large. Therefore, in **Sakamoto**, it is difficult to provide a semiconductor device having high speed operation.

With respect to claims 3 and 4, it is admitted in the Office Action that **Sakamoto** fails to teach the exact amount of carbon in the base layer. It is alleged, however, that **Saito et al.** discloses a semiconductor device layer of SiGe containing carbon, where the layer contains carbon by 0.01% to 60. Such a teaching, however, does not overcome the deficiency of **Sakamoto**, as neither reference nor their combination teaches or suggests a semiconductor device where only the base layer is connected to the first semiconductor layer in the base region, as now called for in Applicant's amended claims.

In view of the present amendments to the claims and the above remarks, it is believed that claims 1-4 and 7-15 are patentable and allowable in addition to allowed claims 5, 6 and 16-20. Early action towards allowance thereof is respectfully requested.

In the event that any fees are due in connection with this paper, please charge our Deposit Account No. 01-2340.

Respectfully submitted,

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